CLAIMS

1. A drive device comprising:

a first generation section for sequentially turning k first signals from a non-output state to an output state according to a first clock, where k is a natural number;

a second generation section for sequentially turning m second signals from the non-output state to the output state according to a second clock, where m is a natural number; and

(k×m) output circuits divided into k groups,

wherein m output circuits belong to each of the k groups,

the k first signals correspond to the k groups,

the m second signals correspond to the m output circuits belonging to each of the k groups, and

each of the (k×m) output circuits:

outputs its corresponding second signal when the second signal is turned to the output state if the first signal corresponding to the group to which the output circuit belongs is in the output state, and

does not output its corresponding second signal even when the second signal is in the output state if the first signal corresponding to the group to which the output circuit belongs is in the non-output state.

2. The drive device of Claim 1, wherein the second generation section sequentially turns the m second signals from the non-output state to the output state according to the second clock during the time when any one of the k first signals is in the output state.

3. The drive device of Claim 1, wherein each of the (k×m) output circuits includes:

an output terminal;

a first input terminal for receiving the second signal corresponding to the output

circuit;

a first switch connected between the output terminal and the first input terminal for switching ON/OFF according to the state of the first signal corresponding to the output circuit;

a second input terminal for receiving a predetermined voltage corresponding to the non-output state of the second signal, and

a second switch connected between the output terminal and the second input terminal for switching ON/OFF according to the state of the first signal corresponding to the output circuit.

4. The drive device of Claim 1, wherein the first generation section includes k first flipflops connected in series, and

the second generation section includes m second flipflops connected in series.

5. The drive device of Claim 1, further comprising a logic circuit connected between the first generation section and the (k×m) output circuits and receiving an external control signal,

wherein the logic circuit turns all of the k first signals from the first generation section to the non-output state simultaneously according to existence/absence of the control signal.

6. The drive device of Claim 1, further comprising a logic circuit connected between the second generation section and the (k×m) output circuits and receiving an external control signal,

wherein the logic circuit turns all of the m second signals from the second generation section to the non-output state simultaneously according to existence/absence of the control signal.

7. The drive device of Claim 4, further comprising:

a first selector connected between the s-th first flipflop from the top and the (s+1)th first flipflop among the k first flipflops, where s is a natural number and $1 \leq s < (k-2)$; and

a second selector connected between the t-th first flipflop from the top and the (t+1)th first flipflop among the k first flipflops, where t is a natural number and $s < t \leq (k-1)$,

wherein the first and second selectors have first and second modes,

in the first mode, the first selector outputs an output from the s-th first flipflop to the (s+1)th first flipflop, and the second selector outputs an output from the t-th first flipflop to the (t+1)th first flipflop, and

in the second mode, the first selector outputs the output from the s-th first flipflop to the second selector, and the second selector outputs an output from the first selector to the (t+1)th first flipflop.

8. The drive device of Claim 4, further comprising:

a selection circuit having first and second modes,

wherein in the first mode, the selection circuit outputs an output from the y-th second flipflop from top among the m second flipflops as the y-th second signal, where y is an odd natural number and m is an even natural number, where $1 \leq y \leq (m-1)$, and outputs an output from the (y+1)th second flipflop as the (y+1)th second signal, and

in the second mode, the selection circuit outputs the output from the y-th second flipflop as the y-th and (y+1)th second signals, and does not output the output from the (y+1)th second flipflop.

9. The drive device of Claim 1, further comprising a logic circuit connected between the first generation section and the (k×m) output circuits and receiving an external control signal,

wherein the logic circuit turns all of the k first signals from the first generation section to the output state simultaneously according to existence/absence of the control

signal.

10. The drive device of Claim 1, further comprising a logic circuit connected between the second generation section and the (k×m) output circuits and receiving an external control signal,

wherein the logic circuit turns all of the m second signals from the second generation section to the output state simultaneously according to existence/absence of the control signal.

11. The drive device of Claim 1, further comprising a logic circuit connected between the first generation section and the (k×m) output circuits and operating according to existence/absence of an external control signal,

wherein the control signal is output for a predetermined duration in the time period from the time when any one of the m second signals is turned to the output state until the time when the next second signal is turned to the output state, the predetermined duration being shorter than the time period, and

once receiving the control signal, the logic circuit turns all of the k first signals from the first generation section to the non-output state simultaneously.

12. The drive device of Claim 1, further comprising a logic circuit connected between the second generation section and the (k×m) output circuits and operating according to existence/absence of an external control signal,

wherein the control signal is output for a predetermined duration in the time period from the time when any one of the m second signals is turned to the output state until the time when the next second signal is turned to the output state, the predetermined duration being shorter than the time period, and

once receiving the control signal, the logic circuit turns all of the m second signals from the second generation section to the non-output state simultaneously.

13. The drive device of Claim 1, further comprising a logic circuit connected between the first and second generation sections and the (k×m) output circuits and receiving an external control signal,

wherein the logic circuit turns all the k first signals from the first generation section to the output state simultaneously and also turns all the m second signals from the second generation section to the output state simultaneously, according to existence/absence of the control signal.

14. The drive device of Claim 3, wherein each of the (k×m) output circuits receives an external control signal, and

the device further comprises a selection section for outputting either the signal supplied at the output terminal or a predetermined voltage corresponding to the output state of the second signal.

15. A drive method for sequentially outputting drive signals from (k×m) output terminals divided into k groups, where k and m are natural numbers, m output terminals belonging to each of the k groups, the method comprising:

sequentially turning k first signals corresponding to the k groups from a non-output state to an output state according to a first clock;

sequentially turning m second signals corresponding to the m output terminals belonging to each of the k groups from the non-output state to the output state according to a second clock; and

in each of the (k×m) output terminals, outputting the second signal corresponding to the output terminal from the output terminal as the drive signal when the second signal is turned to the output state if the first signal corresponding to the group to which the output terminal belongs is in the output state; and

in each of the (k×m) output terminals, not outputting the second signal

corresponding to the output terminal from the output terminal as the drive signal even when the second signal is in the output state if the first signal corresponding to the group to which the output terminal belongs is in the non-output state.